This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Original) A method for forming a structure, the method comprising:

forming a layer over a substrate, the layer having a depletion region having a thickness less than approximately 20 angstroms;

removing a portion of the layer to define a gate of a transistor, the gate defining a channel length;

introducing a plurality of dopants into the substrate proximate the gate to define a source and a drain; and

heating the substrate to a temperature to activate the plurality of dopants,

wherein the temperature is sufficiently low to prevent at least a portion of the plurality of dopants from diffusing enough to induce a high off current.

2. (Original) The method of claim 1 wherein the substrate comprises an insulating layer.

3. (Original) The method of claim 2 wherein the substrate comprises a strained layer disposed over the insulating layer.

4. (Original) The method of claim 1 wherein the substrate comprises a strained layer.

5. (Original) The method of claim 4 wherein the strained layer is tensilely strained.

6. (Original) The method of claim 4 wherein the strained layer is compressively strained.

7. (Original) The method of claim 1 wherein the substrate comprises a relaxed layer.

8. (Original) The method of claim 1 wherein the substrate comprises germanium.

9. (Original) The method of claim 1 wherein the induced off current is less than 10^{-6} Amperes per micrometer.

10. (Original) The method of claim 9 wherein the induced off current is less than 10^{-9} Amperes per micrometer.

11. (Original) The method of claim 1 wherein after the plurality of dopants are introduced, a portion of the plurality of dopants disposed in a region of the source define a source extent proximate the channel, and after heating the substrate, the source extent diffuses under the gate a distance extending less than 12.5% of the channel length.

12. (Original) The method of claim 11 wherein a concentration of the portion of dopants at the source extent is at least approximately 10^{18} atoms/cubic centimeter.

13. (Original) The method of claim 1 wherein after the plurality of dopants are introduced, a portion of the plurality of dopants disposed in a region of the drain define a drain extent proximate the channel, and after heating the substrate, the drain extent diffuses under the gate a distance extending less than 12.5% of the channel length.

14. (Original) The method of claim 13 wherein a concentration of the portion of dopants at the drain extent at least approximately 10^{18} atoms/cubic centimeter.

15. (Original) The method of claim 1 wherein the layer comprises a semiconductor and the step of forming the layer includes introducing a plurality of gate dopants into the layer, and heating the layer to a first temperature to alter a distribution of the gate dopants in the layer.

16. (Original) The method of claim 15 wherein the semiconductor comprises silicon.

17. (Original) The method of claim 1 wherein the semiconductor comprises germanium.

18. (Original) The method of claim 1 wherein the layer comprises a metallic element.

19. (Original) The method of claim 18 wherein the metallic element comprises at least one of molybdenum, titanium, tantalum, tungsten, iridium, nickel, cobalt, and platinum.

20. (Original) A method for forming a structure, the method comprising:

introducing a first plurality of dopants into a gate electrode layer disposed over a substrate;

heating the gate electrode layer to a first temperature to alter a distribution of the first plurality of dopants in the gate electrode layer;

removing a portion of the gate electrode layer to define a gate of a transistor;

introducing a second plurality of dopants into the substrate proximate the gate to define a source and a drain; and

heating the substrate to a second temperature to activate the second plurality of dopants, wherein the second temperature is less than the first temperature.

21. (Original) The method of claim 20 wherein the substrate comprises an insulating layer.

22. (Original) The method of claim 21 wherein the substrate comprises a strained layer disposed over the insulating layer.

23. (Original) The method of claim 20 wherein the substrate comprises a strained layer.

24. (Original) The method of claim 23 wherein the strained layer is tensilely strained.

25. (Original) The method of claim 23 wherein the strained layer is compressively strained.

26. (Original) The method of claim 20 wherein the substrate comprises a relaxed layer.

27. (Original) The method of claim 20 wherein the substrate comprises germanium.

28. (Original) The method of claim 20, wherein the first temperature is greater than 1000 °C.

29. (Original) The method of claim 20, wherein the second temperature is less than 1000 °C.

30. (Original) The method of claim 20 wherein the gate electrode layer comprises a semiconductor layer.

31. (Original) The method of claim 30 wherein the semiconductor layer comprises silicon.

32. (Original) The method of claim 30, wherein the semiconductor layer comprises germanium.

33. (Original) The method of claim 20 wherein the first plurality and the second plurality of dopants comprise n-type dopants.

34. (Original) The method of claim 20 wherein the first plurality and the second plurality of dopants comprise p-type dopants.

35. (Currently amended) A method for forming a structure, the method comprising:

introducing a first plurality of dopants into a gate electrode layer disposed over a substrate;

heating the ~~semiconductor layer~~substrate for a first time period to alter a distribution of the first plurality of dopants in the gate electrode layer;

removing a portion of the gate electrode layer to define a gate of a transistor;

introducing a second plurality of dopants into the substrate proximate the gate to define a source and a drain; and

heating the substrate for a second time period to activate the second plurality of dopants,

wherein the second time period has a shorter duration than a duration of the first time period.

36. (Original) The method of claim 35 wherein the substrate comprises an insulating layer.

37. (Original) The method of claim 36 wherein the substrate comprises a strained layer disposed over the insulating layer.

38. (Original) The method of claim 35 wherein the substrate comprises a strained layer.

39. (Original) The method of claim 38 wherein the strained layer is tensilely strained.

40. (Original) The method of claim 38 wherein the strained layer is compressively strained.

41. (Original) The method of claim 35 wherein the substrate comprises a relaxed layer.

42. (Original) The method of claim 35 wherein the substrate comprises at least one of silicon and germanium.

43. (Original) The method of claim 35 wherein the first time period is greater than 5 seconds.

44. (Original) The method of claim 35 wherein the first time period is greater than 30 seconds.

45. (Original) The method of claim 35 wherein the gate electrode layer comprises a semiconductor layer.

46. (Original) The method of claim 45 wherein the semiconductor layer comprises silicon.

47. (Original) The method of claim 45 wherein the semiconductor layer comprises germanium.

48. (Original) The method of claim 35 wherein the first and the second plurality of dopants comprise n-type dopants.

49. (Original) The method of claim 35 wherein the first and the second plurality of dopants comprise p-type dopants.

50.– 60. (Canceled)

61. (Currently amended) [[The]]A structure ~~of claim 50, further~~ comprising:

a strained layer disposed over a substrate;

a first transistor including:

a first source and a first drain, wherein at least a portion of the first source and a portion of the first drain are disposed in a first portion of the strained layer,

a first gate disposed above the strained layer and between the source and drain, the first gate comprising a first metal, and

a first gate dielectric layer disposed between the first gate and the strained layer; and

a second transistor including:

a second source and a second drain, wherein at least a portion of the second source and a portion of the second drain are disposed in a second portion of the strained layer;

a second gate disposed above the strained layer and between the second source and second drain, the second gate comprising a second metal; and

a second gate dielectric layer disposed between the second gate and the strained layer,

wherein the first transistor is an n-type metal-oxide semiconductor field-effect transistor, the first source and the first drain comprise n-type dopants, the second transistor is a p-type metal-oxide-semiconductor field-effect transistor, [[and]] the second source and second drain comprise p-type dopants, the first gate has a first workfunction, the second gate has a second workfunction, and the first workfunction is substantially different from the second workfunction.

62. – 63. (Canceled)